

**What is claimed is:**

1           1.    A high voltage device comprising:  
2           a substrate of a first type;  
3           a first and second well respectively of the first and a  
4           second type in the substrate;  
5           a gate formed on the substrate;  
6           a first and second doped region both of the second  
7           type, respectively formed in the first and second  
8           well and both sides of the gate; and  
9           a third doped region of the first type in the first  
10          well and adjacent to the first doped region.

1           2.    The high voltage device as claimed in claim 1  
2          further comprising field oxides isolating the high voltage  
3          device from other devices on the substrate.

1           3.    The high voltage device as claimed in claim 1,  
2          wherein the gate comprises a gate oxide on the substrate, a  
3          conducting layer on the gate oxide and spacers on two sides  
4          of the gate oxide and conducting layer.

1           4.    The high voltage device as claimed in claim 3  
2          further comprising a fourth lightly doped region of the  
3          second type adjacent to the first doped region and beneath  
4          one of the spacers.

1           5.    The high voltage device as claimed in claim 1,  
2          wherein there is a spacing of the second doped region to the  
3          gate.

1        6.    The high voltage device as claimed in claim 1,  
2    wherein the overlay of the gate and the second well is  
3    defined as zero.

1        7.    The high voltage device as claimed in claim 1,  
2    wherein the first and second types are respectively P and N  
3    type.

1        8.    The high voltage device as claimed in claim 1,  
2    wherein the first and second type are respectively N and P  
3    type and the high voltage device further comprises a N+  
4    buried layer in the substrate and beneath the first and  
5    second well.

1        9.    A high voltage device formed on a P substrate  
2    comprising:

3        an HVNMOS comprising:

4            a first P and N well in the P substrate;  
5            a first gate formed on the P substrate;  
6            two first N+ doped regions respectively formed in  
7            the first P and N well, and both sides of  
8            the first gate; and

9            a first P+ doped region in the first P well and  
10           adjacent to the first N+ doped region in the  
11           first P well; and

12        a HVPMOS comprising:

13           an N+ buried layer in the P substrate;  
14           a second N and P well in the P substrate and above  
15           the N+ buried layer;  
16           a second gate formed on the P substrate;

17           two second P+ doped regions respectively formed in  
18           the second N and P well, and both sides of  
19           the second gate; and  
20           a second N+ doped region in the second N well and  
21           adjacent to the second P+ doped region in  
22           the second N well.

1           10. The high voltage device as claimed in claim 9  
2 further comprising field oxides isolating the HVPMOS and  
3 HVNMOS from other devices on the P substrate.

1           11. The high voltage device as claimed in claim 9,  
2 wherein each of the first and second gates comprise a gate  
3 oxide on the P substrate, a conducting layer on the gate  
4 oxide and spacers on both sides of the gate oxide and  
5 conducting layer.

1           12. The high voltage device as claimed in claim 11,  
2 wherein the HVNMOS further comprises an N lightly doped  
3 region adjacent to the first N doped region in the first P  
4 well and beneath one of the spacers of the first gate, and  
5 the HVPMOS further comprises a P lightly doped region  
6 adjacent to the second P doped region in the second N well  
7 and beneath one of the spacers of the second gate.

1           13. The high voltage device as claimed in claim 9,  
2 wherein there is spacing of the first N+ doped region in the  
3 first N well to the first gate and the second P+ doped  
4 region in the second P well to the second gate.

1           14. The high voltage device as claimed in claim 9,  
2 wherein the overlay of the first gate and the first P well,

3 and the second gate and the second N well are defined as  
4 zero.

1 15. A method for manufacturing a high voltage device,  
2 comprising the steps of:  
3 providing a substrate of a first type;  
4 forming a first and second well respectively of the  
5 first and a second type in the substrate;  
6 forming a gate on the substrate;  
7 forming a first and second doped region both of the  
8 second type, respectively in the first and second  
9 well and both sides of the gate; and  
10 forming a third doped region of the first type in the  
11 first well and adjacent to the first doped  
12 region.

1 16. The method as claimed in claim 15 further  
2 comprising the step of:  
3 forming field oxides isolating the high voltage device  
4 from other devices on the substrate.

1 17. The method as claimed in claim 15, wherein the  
2 gate comprises a gate oxide on the substrate, a conducting  
3 layer on the gate oxide and spacers on two sides of the gate  
4 oxide and conducting layer.

1 18. The method as claimed in claim '17 further  
2 comprising the step of:  
3 forming a fourth lightly doped region of the second  
4 type adjacent to the first doped region and  
5 beneath one of the spacers.

1        19. The method as claimed in claim 15, wherein there  
2 is a spacing of the second doped region to the gate.

1        20. The method as claimed in claim 15, wherein the  
2 overlay of the gate and the second well is defined as zero.

1        21. The method as claimed in claim 15, wherein the  
2 first and second type are respectively P and N type.

1        22. The method as claimed in claim 1, wherein the  
2 first and second type are respectively N and P type and the  
3 method further comprises the step of:

4        forming an N+ buried layer in the substrate and beneath  
5                the first and second well.

1        23. A method for manufacturing a high voltage device  
2 comprising the steps of:

3        providing a P substrate;

4        forming a HVNMOS on the P substrate by:

5                forming a first P and N well in the P substrate;

6                forming a first gate on the P substrate;

7                forming two first N+ doped regions respectively in  
8                        the first P and N well, and both sides of  
9                        the first gate; and

10                forming a first P+ doped region in the first P  
11                        well and adjacent to the first N+ doped  
12                        region in the first P well; and

13        forming a HVPMOS on the P substrate by:

14                forming an N+ buried layer in the P substrate;

15                forming a second N and P well in the P substrate  
16                        and above the N+ buried layer;

17           forming a second gate on the P substrate;  
18           forming two second P+ doped regions respectively  
19                 in the second N and P well, and both sides  
20                 of the second gate; and  
21           forming a second N+ doped region in the second N  
22                 well and adjacent to the second P+ doped  
23                 region in the second N well.

1           24. The method as claimed in claim 23 further  
2     comprising the step of:

3           forming field oxides isolating the HVPMOS and HVNMOS  
4                 from other devices on the P substrate.

1           25. The method as claimed in claim 23, wherein each of  
2     the first and second gate comprises a gate oxide on the P  
3     substrate, a conducting layer on the gate oxide and spacers  
4     on both sides of the gate oxide and conducting layer.

1           26. The method as claimed in claim 25 further  
2     comprising the steps of:

3           forming a N lightly doped region adjacent to the first  
4                 N doped region in the first P well and beneath  
5                 one of the spacers of the first gate; and  
6           forming a P lightly doped region adjacent to the second  
7                 P doped region in the second N well and beneath  
8                 one of the spacers of the second gate.

1           27. The method as claimed in claim 23, wherein there  
2     is spacing of the first N+ doped region in the first N well  
3     to the first gate and the second P+ doped region in the  
4     second P well to the second gate.

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- 1        28. The method as claimed in claim 23, wherein the
- 2        overlay of the first gate and the first P well, and the
- 3        second gate and the second N well are defined as zero.